

TID Test on 16 Mbit Flash Memories

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Abstract -- In this paper we analyze the failures of Commercial Off The Shelf (COTS) 16 Mb Flash memories in radiation environment. The experimental set-up, the test procedure, and the results of a Cobalt-60 exposure performed in the Calliope facility at the E.N.E.A. Casaccia laboratories are described in some details. A Total Ionizing Dose (TID) up to 30 krad was experimented on devices in unbiased and dynamically biased conditions. Irradiation, test, annealing, and ageing have been performed according to ESA specifications.

Functionality test has been performed at several steps together with single cell current sink statistics, standby supply current sink, and I/O pins current sink measurement. Moreover a measurement of supply current during operation was accomplished using custom electronics.

Index Terms -- COTS, Flash memories, Space environment, TID.

I. INTRODUCTION

THE storage of large amount of data is a very important issue in space applications. Until few years ago, the common memories were the tape recorders. Since 16 Mb DRAM appeared on the market, Solid State Mass Memories (SSMM) are replacing the old electro-mechanical devices. Nowadays different kinds of memory devices such as Flash memories are becoming available [1], [2].

Flash devices could be very promising for applications that need long-term data retention with very low power consumption as in the case of satellite hibernation. Also systems where a power or a refresh mechanism failure should not result in a loss of data can take advantage from this technology.

For these reasons, we are studying the behavior of these devices in radiation environment both to evaluate feasibility of SSMM based on this technology and to provide system or technological solutions to improve their resistance to radiation effects.

These tests are part of a larger program. Other tests are scheduled at different facilities to study heavy ions effects.

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These efforts are aimed to the implementation of a SSMM based either on SDRAM or Flash components.

Section 2 presents the test plan and in section 3 an overview of the experimental setup is presented. Section 4 contains the results obtained at the Calliope facility in the E.N.E.A. Casaccia laboratories (Rome, Italy). A description of future development of this work is given in section 5.

II. THE TESTING PROCEDURE

These tests are dedicated to the characterization of ST Microelectronics (STM) 16 Mb Flash memories response to TID [3], [4]. The DUTs have been irradiated to a total dose of 30.6 krad with four intermediate steps at 3.4, 10.2, 20.4 krad. The tests have been performed according to ESA/SCC 22900 [5], [6] specifications whose main features are:

- Total dose test should be performed with a ^{60}Co γ -ray source with a dose rate between 3.6 to 36 krad/h and dose rate accuracy should be within 5%;
- Intermediate steps for measurements should have a maximum time of 2 hours;
- Temperature should be 20 ± 10 °C during exposure and testing;
- Exposure should be performed with components under bias.
- After the irradiation, components should be tested and annealed for 168 hours with measurement after 12, 24, 168 hours.
- After annealing, ageing has to be performed by baking components at their maximum operating temperature under bias for 168 hours with no stops. At the end the final characterization has to be performed.

After each exposure step the response of memory devices to radiation were determined by the following measurements:

- Supply current in stand-by;
- Electrical current sink of all the device I/O pins;
- Electrical current sink of memory cell in a large memory block;
- Device logic failure;
- Measurement of the supply current sink in operation mode (Read, Writes, and Erase).

In order to obtain the worst-case damage, the devices were biased under radiation.

In addition, some devices were exposed without biasing in order to appreciate the different effects of radiation.

III. THE EXPERIMENTAL SET-UP

Both exposure and measurement have been performed at the Calliope facility at the Casaccia laboratory of E.N.E.A. (Rome, Italy).

Calliope is a pool type irradiation plant equipped with a ^{60}Co γ -ray source. The source is located in the middle of a large (7x6x3.9 m) shielded room having 1.8 m thick baritic concrete walls. The emitted radiation is composed of two photons of 1.173 and 1.332 MeV emitted in coincidence (average 1.25 MeV). Actually, the activity of the source is 67.8 kCi but the plant is licensed up to 100 kCi. The possible dose rates range from few tens of rad/h up to 2 Mrad/h. Dosimetry is performed with three different dosimeters:

- Fricke solution (2-20 krad);
- Alanine (0.1-100 krad);
- Red Perspex (0.5-4 Mrad).

A number of 24 STM M28W160T COTS devices have been irradiated. The chips were plugged into Zero Insertion Force (ZIF) sockets of a board shielded with 2 mm of aluminum in order to provide charged particles equilibrium. This board was connected to a custom control board based on a Complex Programmable Logic Device (CPLD) in order to provide stimuli, which dynamically bias the DUTs at a state frequency of 10 MHz.

A custom circuit, on the control board, monitored supply current and a digital oscilloscope acquired the waveforms. The control board stayed in the hot-room shielded with a 5 cm lead wall.

Sixteen DUTs were dynamically biased with Erase, Write, and Read operations. Four DUTs were continuously read, statically biased and unbiased respectively.

Supply current monitor was performed on two devices per bias type.

At the end of each step the board was moved to a laboratory in the same plant and the devices were unplugged and characterized with a Credence Kalos-XP-KPDS integrated circuit tester.

Annealing and ageing were performed on four DUTs in the U.L.I.S.S.E. Consortium laboratories in Rome.

IV. THE RESULTS

A. Memory cell current sink test

This test uses device built-in test mode, named Direct Memory Access (DMA). The DMA allows the measurement of the drain current I^R for each memory cell. The cell current sink was measured on 7744 cells per device per 20 devices. All measured cells were erased. The acquired data for each exposure step are reported in Fig. 1. In order to verify the device functionality at the end of each measurement step Write, Erase and Read cycles were done. As shown in Fig. 1 the distribution was moved to lower current by radiation.

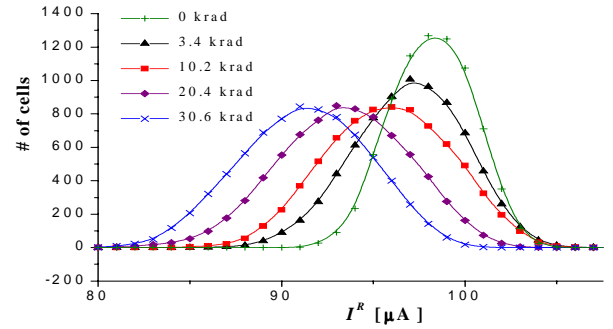


Fig. 1. Distribution of cells vs. current over tested devices at each exposure step.

The plot in Fig. 2 is obtained considering I^R as the average of the devices mean current.

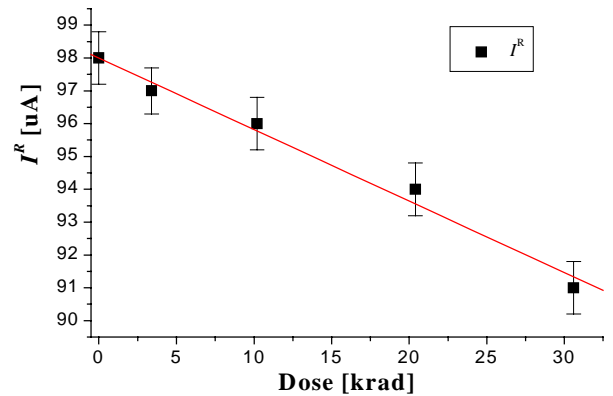


Fig. 2. Cell current sink vs. ionizing dose.

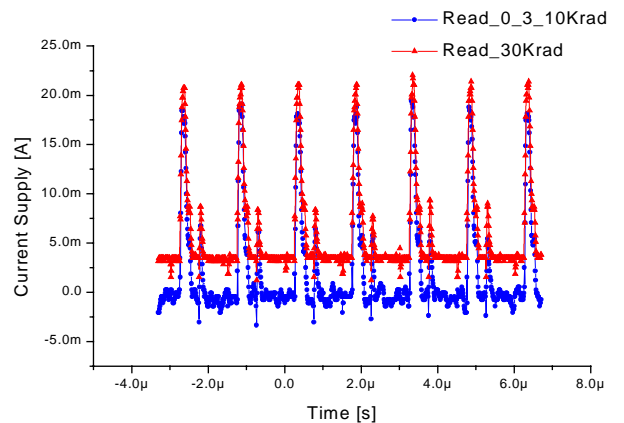


Fig. 3. The supply current during Read operation.

B. Supply current measurement

A supply current measurement during operation was performed using custom electronics. Some devices were monitored: the supply current sink was both observed during

all the experiment and recorded at the main radiation step. Figure 3 shows the increase of the current due to the radiation during a DUT read. Similar results were observed in other monitored devices.

In Fig. 4 is shown the device RMS supply current sink in Read, Write and Erase operations vs. dose. The values are calculated integrating the ICC waveform digitally acquired. Particular care was devoted to keep the same triggering condition at every acquisition. It is possible to notice that the dose causes a rise in the current absorbed in every operation.

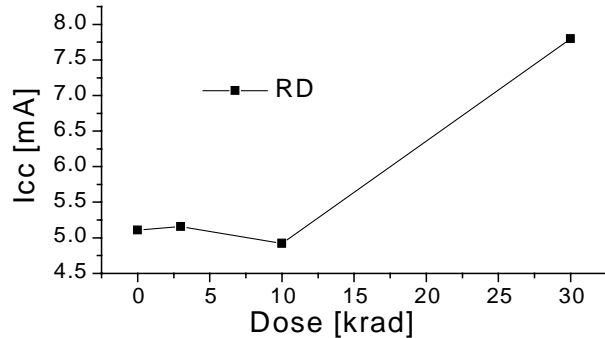


Fig. 4. The RMS supply current during Read operation.

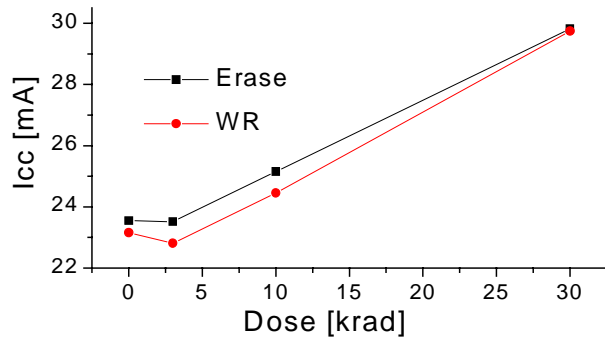


Fig. 5. The RMS supply current during Write and Erase operation.

C. Supply standby current test

Figure 6 shows the behavior of the mean standby supply current of both biased and unbiased devices when the dose increases. Since the large grow of the leakage current, the last point of biased devices is affect by an error because of saturation of measurement system.

D. Logic failure test

All the devices tolerated 20.4 krad without logic failure. Erase, write and read operation were correctly performed even if the time necessary to carry out erase and write increased of about 20%.

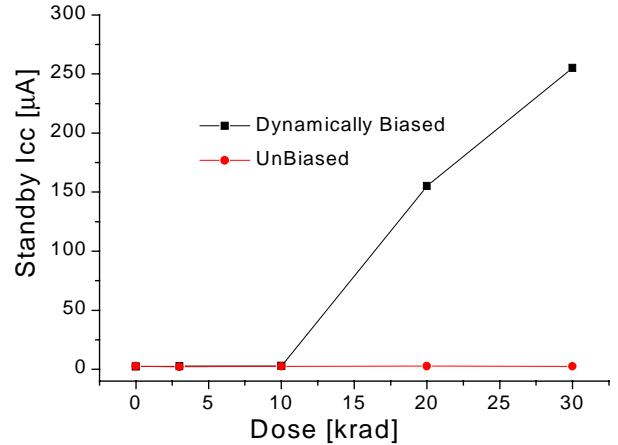


Fig. 6 Mean standby supply current vs. ionizing dose.

After 30.6 krad, 14 of the 16 dynamically biased devices and two of the statically supplied showed failure in the erase operation.

On the contrary, all the unbiased devices continued to operate correctly.

Both annealing and ageing did not change this result.

V. CONCLUSIONS AND FUTURE WORK

An overview of test equipment and procedures are presented in order to investigate 16 Mb Flash devices in ionizing environment. Complete results of test performed on memory cell in DMA mode are presented in details together with measurement of supply current at different dose level and in different operating and biasing condition.

The next step of our program is to perform Single Event Effects (SEE) tests [7]. For this purpose a test system has been developed to perform SEE test in different heavy ions facility. A preliminary SEE test was performed at GSI laboratories and other tests are planned in INFN Legnaro and Catania facilities.

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VII. REFERENCES

- [1] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells-an overview," *Proc. of the IEEE*, vol. 85, n. 8, pp. 1248-1271, 1997.
- [2] R. Bez, et al., *IEEE Electron Device Letters* Vol.19 N.2 Feb. 1998 pp. 37-39.
- [3] A. K. Sharma, K. Sahu, "Characterization of commercial high density memories under low dose rate total ionizing dose (TID) testing for nasa programs," *Proc. of IEEE Radiation Effects Data Workshop*, pp. 90-96, 1997.
- [4] D. N. Nguyen, S. Guertin, G. M. Swift, and A. H. Johnston, "Radiation Effects on Advanced Flash Memories", Jet Propulsion Laboratory California Institute of Technology Pasadena, California, 1999.

- [5] Space Components Coordination Group (SCC), European Space Agency (ESA), "Total Dose Steady-State Irradiation Test Method," ESA/SCC Basic Specifications n. 22900.
- [6] P. S. Winokur, et al., "Advanced Qualification Techniques," *IEEE Trans. on Nuclear Science*, vol. 41, n. 3, pp. 538-548, 1997.
- [7] H. R. Schwartz, D. K. Nichols, A. H. Johnston, "Single-Event Upset in Flash Memories," *IEEE Trans. on Nuclear Science*, vol. 44, n. 6, pp. 2315-2324, 1997.
- [8] S. Bertazzoni, G. C. Cardarilli, G. C. Grande, D. Piergentili, M. Salmeri, S. Sperandei, "Tests of 64 Mb SDRAM for Space Applications," *Proc. of European Conference on Circuit Theory and Design, ECCTD 99*, Stresa, Italy, August 29 - September 2, 1999.
- [9] S. Bertazzoni, G. C. Cardarilli, D. Di Giovenale, G. C. Grande, D. Piergentili, M. Salmeri, A. Salsano, S. Sperandei, "Failure Tests on 64 Mb SDRAM in Radiation Environment," *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, DFT 99*, Albuquerque, New Mexico, USA, November 1-3, 1999.