TID Test for SDRAM Based IEEM Calibration System

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***Abstract*— Traditionally, to map out device sensitivity with submicrometric resolutions one uses a microbeam. Ion Electron Emission Microscopy (IEEM) appears to be a promising new method for device characterization. An advanced implementation of this instrument is under development at the SIRAD irradiation facility of the Legnaro National Laboratory (LNL). In IEEM operations Total Integrated Dose (TID) effects could be a potential problem and should be addressed before the final test. For this purpose a TID monitoring method, based on the measurement of the bit retention time, that is the time the information is retained in a memory cell without refresh, in Synchrous Dynamic RAM (SDRAM) Commercial Off The Shelf (COTS) devices, is proposed. This paper presents the experimental setup and the results of a preliminary TID test with a ^{60}Co gamma ray source on SDRAM COTS to test the method.**

***Index Terms*— IEEM, TID, SDRAM, COTS.**

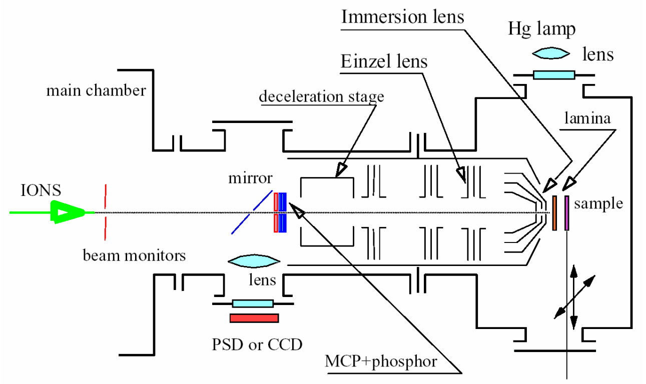

Fig. 1. IEEM configuration

I. INTRODUCTION

Device sensitivity is usually mapped out with submicrometric resolutions using a microbeam facility. In recent times Ion Electron Emission Microscopy (IEEM) has entered the scene and appears to be a promising method for device characterization [1]. An advanced implementation of this instrument is under development at the SIRAD irradiation facility located at the XTU Tandem of the of the Legnaro National Laboratories (LNL) [2]–[4].

In Fig. 1 the axial IEEM configuration developed at the LNL.

At the end of its development stage the SIRAD IEEM needs to be tested with a real microelectronic device to demonstrate the IEEM capabilities, in particular measure the effective spatial resolution in device sensitivity micromapping. The performance of the IEEM will be tested in an experiment with Synchronous Dynamic RAM (SDRAM) Commercial Off The Shelf (COTS) devices since they are a well known and have suitable characteristics.

In IEEM operations Total Ionizing Dose (TID) effects due ions impact could be a potential problem and need to be addressed in an independent way before the final IEEM tests. In particular it is important to monitor the TID aging effect during the experiment since it could affect the results. For this purpose a TID monitoring method based on the measurement of the bit retention time (i.e. the time the information is retained in a memory cell without refresh) is proposed.

This paper presents the experimental setup and the results of a preliminary TID test with a ^{60}Co gamma ray source on SDRAM COTS [5], [6] to test the method. This test, performed on different SDRAM chips at the LNL of the National Institute for Nuclear Physics, demonstrates the feasibility of a TID monitoring system based on the measurement of SDRAM retention time. The proposed TID monitoring method could be easily implemented in a SDRAM controller to supervise the TID effects on SDRAM used in systems working in radiation environments.

II. TOTAL IONIZING DOSE TEST

The effects of Total Ionizing Dose have been investigated on Micron 256 Mb MT48LC32M8A2Y96A SDRAM devices not enclosed in their case and directly bonded onto suitable carriers. Overall, four devices have been irradiated. Two of them have been constantly keep under operation, while the other two have been irradiated and characterized only before and after the exposure.

The gamma ray source utilized consists of a ^{60}Co cylindrical core lodged in a case full of shielding pellets. ^{60}Co decays in β^- and produces two γ photons with energies 1.173210 and 1.332470 MeV with an efficiency near 100%. An automatic mechanism, driven from the outside of the irradiation bunker, extracts the source from its case allowing the exposure of the

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devices under test (DUT) placed on a large rectangular table. The dose rate at 30 cm from the source and behind a 2.5 mm Al shield, is 2.7 rad(Si) s^{-1} (about 10 krad(Si) h^{-1}) with an uniformity better than 10% over the whole DUT area.

The test consisted of two sequential irradiation sessions of 50 krad and 20 krad respectively for a total dose of 70 krad and monitoring the exposed memory cells logic state measuring the number of cells which shown a logic state change vs. the latency time, that is the time between the cell write operation and the following reading of their value, in the range between about 50 ms and about 30 s. This test has been performed during the exposure at regular predefined dose intervals (about 10–15 krad).

III. TEST PROCEDURE

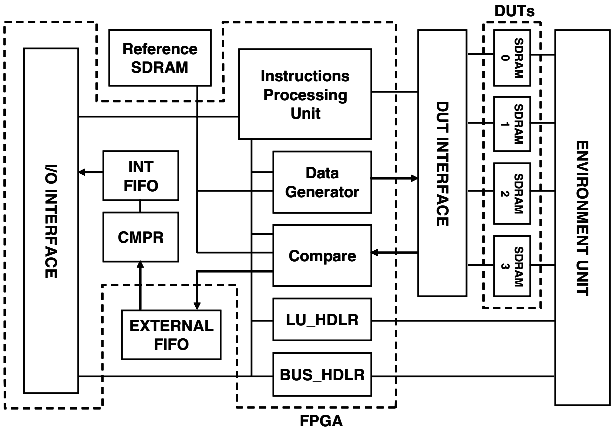

Fig. 2. Test Board scheme

In order to test SDRAM cells, a custom Test Board, shown in Fig. 2, has been developed and implemented. In order to achieve the maximum performance allowed by the SDRAM advanced input-output features (burst mode, self refresh), the Test Board (TB) was developed using a FPGA. The system core mapped on the FPGA is the Memory Control module that is able to handle read, write and refresh operations plus complex test procedures as:

- Write an internally generated pattern on block cell.
- Read a block of cells.
- Compare a block of cells.

The compare operation is the basis for all the test procedures; in fact the status of the DUT (Hot-DUT) is checked by comparing the content of its cells with the corresponding ones of a reference device (Cold-DUT). The results of the compare operation, which is performed in burst mode at the full speed of the hardware, are stored in a FIFO; a compression procedure is then performed in order to transmit only the information on the differences to the Test Control PC (TCPC) (see Fig. 3). The communication between TB and TCPC is obtained by a Client-Server scheme, which allows TCPC to remotely drive the test. The RABBIT microprocessor is connected to the TB I/O interface and supports TCP-IP Ethernet connection towards TCPC. A dedicated software is loaded in the microprocessor flash memory to manage the communication on TCP-IP protocol and to correctly drive the TB.

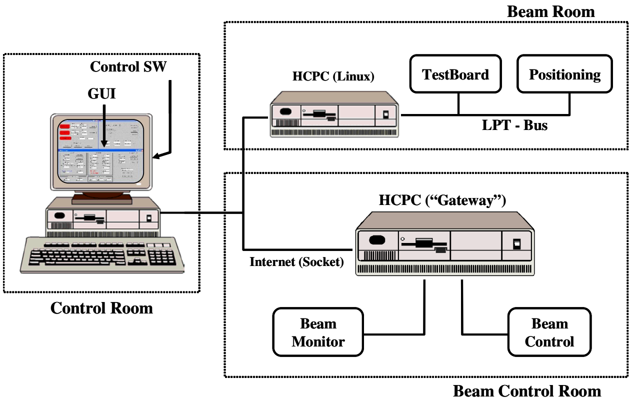

Fig. 3. System scheme

On the TCPC runs the software procedure which controls the test. The test flow is presented in Fig. 4.

The test cycle starts initializing test parameters and writing both the irradiated device (Hot DUT - HDUT) and the reference, not irradiated, device (Cold DUT - CDUT) with the same test pattern defined as

$$DATA(R,C) = \{(R + SEED)[3:0], (C + SEED)[3:0]\}$$

where: $SEED$ is a test parameter used to have a different pattern a each iteration; R is the Row address; C is the Column address. After the writing operation some spy cells are inserted in the HDUT and the device undergo a preliminary test routine to verify the write operation and to count the number of errors at the beginning of the test. If the write operation is successful the refresh is stopped until the Discharge Time (DT) is elapsed. At that time the refresh is restarted and the test routine is performed to count the cells that lose the stored information after the time DT. Then DT is incremented of DTS (DT Step) and a new test iteration is performed until DT is less than DTMAX. After a test cycle the procedure is suspended until the device accumulate TID for a time CD (Cycle Delay) in realistic refresh conditions. The test stop at the end of irradiation.

IV. RESULTS

The analysis of the test data emphasizes the following interesting effects.

1) A gradual reduction of the data retention time proportional to the absorbed dose (Fig. 5 and 6). This evident effect allows us to establish a direct relation between the number of the errors and the absorbed dose (Fig. 7).
2) An immediate increase of the number of errors during irradiation (Fig. 6, curve 50 krad Off and 50 krad On). This effect originates from charge injection in the depletion regions by incident ionizing radiation, which produces leakage currents that alters the amount of charge

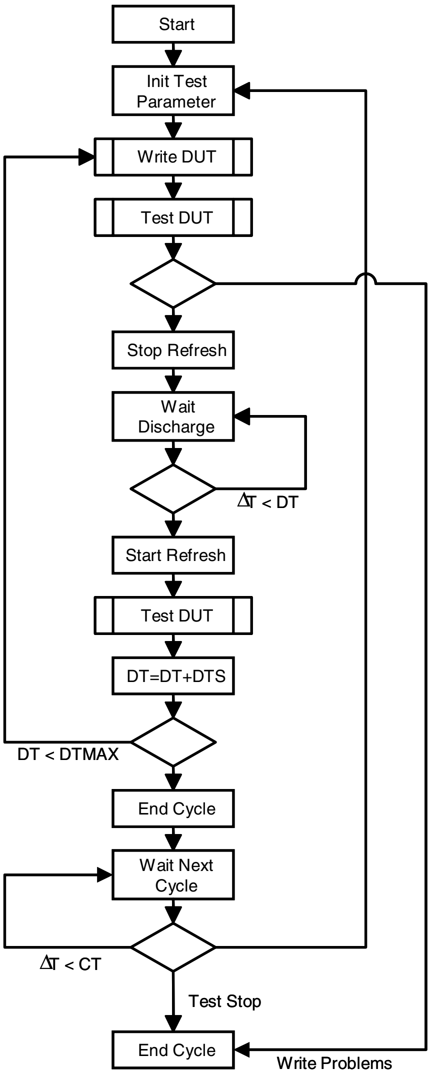

Fig. 4. Algorithm flow

and hence the cell state. Moreover, this effect suggests a method for dose rate measurements.

3) An annealing effect that causes a noticeable degradation of the performance of the devices during the their life (Fig. 8).
4) At last, comparing the data with those measured after 72 h the exposure (Fig. 9), clearly shows the decisive role of the bias voltages applied to the device during the exposure. In fact, because the voltages hinder the recombination of the $e-h$ couples produced in the device by the radiation, they amplify the radiation effects.

V. CONCLUSIONS

This paper proposes a monitoring method to measure online the degradation of SDRAM devices due to Total Ionizing Dose. The method is based on the simple measurement of the bit retention time that can be performed on most systems, based on SDRAM devices, without hardware modification and minimum software enhancement. In particular, the analysis of the test data shows a linear reduction of the data retention time proportional to the absorbed dose. This effect allows us to measure the absorbed dose starting from the number of the corrupted memory cells. The tests performed on MT48LC32M8A2Y96A SDRAMs with a ^{60}Co gamma ray source show that these devices resist 50 krad of TID without evident damage so that they are compatible with IEEM tests.

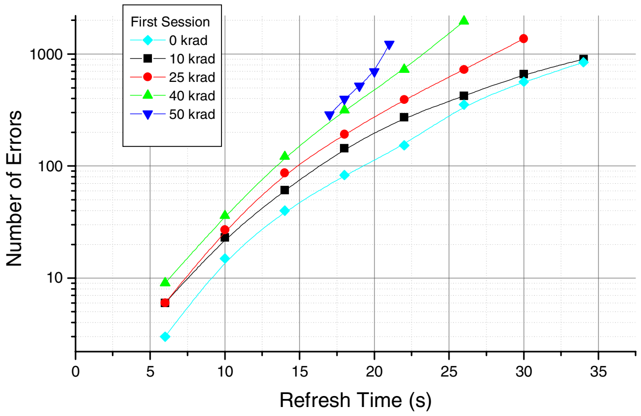

Fig. 5. Number of errors vs. the refresh time in the 1st test session

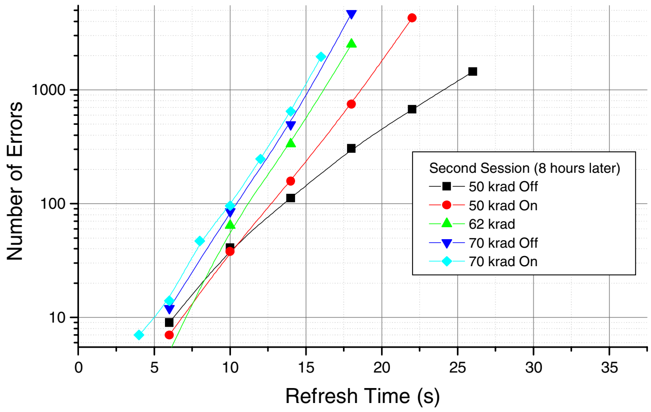

Fig. 6. Number of errors vs. the refresh time in the 2nd test session

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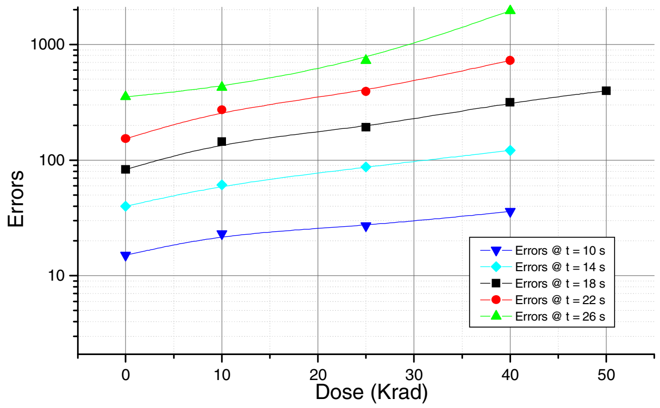

Fig. 7. Relation between the number of errors and the absorbed dose

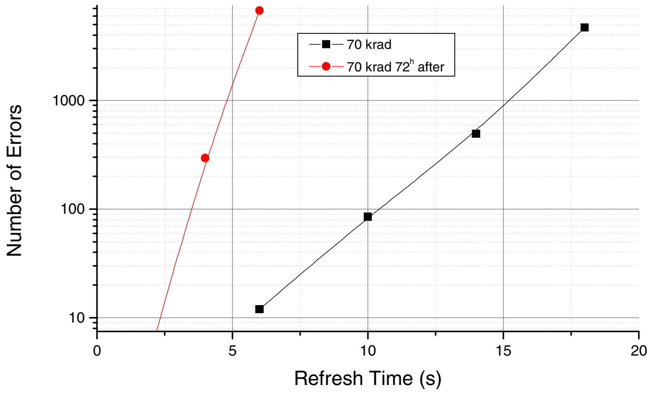

Fig. 8. Device degradation due to the annealing

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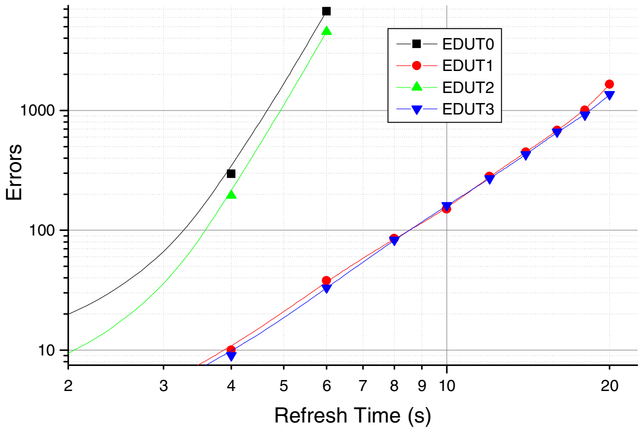

Fig. 9. Bias voltage effect during the exposure