Monitoring methodology for TID damaging of SDRAM devices based on retention time analysis

S. Bertazzoni, D. Di Giovenale, M. Salmeri, A. Mencattini, A. Salsano, M. Florean,
Dept. of Electronic Engineering
University of Rome "Tor Vergata"
Via del Politecnico 1, 00133 Roma, Italy
bertazzoni@ing.uniroma2.it

J. Wyss,
INFN Sezione di Pisa
Via Livornese 1291, 56010 San Piero a Grado (PI), Italy
wyss@unicas.it

R. Rando,
INFN Sezione di Padova
Via Marzolo 8, 35131 Padova, Italy
rando@pd.infn.it

S. Lora
Consiglio Nazionale delle Ricerche
Istituto per la Sintesi Organica e la Fotoreattività
Via P. Gobetti 101, 40129 Bologna, Italy
lora@isof.cnr.it

Abstract

Total Ionizing Dose (TID) is a potential problem for solid state devices exposed to ionizing radiations. An important parameter to define is the level of TID the device can tolerate. This value is very useful in order to predict its operative life time in a radiation environment. In this paper an online monitoring method to measure the degradation of Synchronous Dynamic RAM (SDRAM) Commercial Off The Shelf (COTS) devices due to TID is proposed. The method is based on the measurement of the bit retention time, that is the time the information is retained in a memory cell without refresh. This approach is based on the observation that on same die, a dispersion of the devices' characteristics exist. So, the device degradation will appear in a more evident way in those memory cells having worst electrical characteristics. For this reason, there is a gradual increment of the number of memory cells that do not maintain their initialization value with the increment of the absorbed dose.

The proposed method is useful to monitor the real level of degradation of a SDRAM device in order to optimize maintenance activity and graceful performance degradation techniques. SDRAM devices are used as a TID radiation detector to monitor the real dose absorbed by itself, and thus by the whole apparatus. The method is based on functional test that a SDRAM controller can easily perform on empty memory blocks without requiring dedicated hardware.

This paper presents the experimental setup and the results of a preliminary TID test with a ^{60}Co gamma ray source on SDRAM COTS to validate the method.

1. Introduction

Total Ionizing Dose (TID) is a potential problem for solid state devices exposed to ionizing radiations [1–4]. In order to predict the operative life time of a certain solid state device working in a radiation environment the level of TID the device can tolerate must be measured.

In this paper an online monitoring method to measure the degradation of Synchronous Dynamic RAM (SDRAM) Commercial Off The Shelf (COTS) devices due to TID is proposed. The method is based on the measurement of the bit retention time, that is the time the information is retained in a memory cell without refresh. The proposed method is useful for the following reasons.

1. To improve standard preliminary tests with information useful to implement graceful performance degradation techniques.

2. To monitor the real level of degradation of a SDRAM device in order to optimize maintenance activity.
3. To monitor the real TID a SDRAM, and consequently the apparatus, absorbed using SDRAM devices like a TID radiation detector.

This paper presents the experimental setup and the results of a preliminary TID test with a ^{60}Co gamma ray source on SDRAM COTS to test the method. This test, performed on different SDRAM chips at the CNR irradiation facility of the Legnaro National Laboratory (LNL) of the National Institute for Nuclear Physics, demonstrates the feasibility of a TID monitoring system based on the measurement of SDRAM retention time. The proposed TID monitoring method could be easily implemented in a SDRAM controller to supervise the TID effects on SDRAM used in systems working in radiation environments.

2. TID test

The gamma ray source was a ^{60}Co cylindrical core[1] lodged in a case full of shielding pellets. ^{60}Co decays in β^- and produces two γ photons with energies 1.173210 and 1.332470 MeV with an efficiency near 100%. An automatic mechanism, driven from the outside of the irradiation bunker, extracts the source from its case allowing the exposure of the devices under test (DUT) placed on a large rectangular table. The dose rate at 30 cm from the source and behind a 2.5 mm Al shield, is 2.7 rad(Si) s^{-1} (about 10 krad(Si) h^{-1}) with an uniformity better than 10% over the whole DUT area.

Figure 1 shows the whole algorithm used in order to gather the desired data for the SDRAM characterization.

The test procedure begins initializing parameters and writing both the irradiated device (Hot DUT-HDUT) and a reference not irradiated device (Cold DUT-CDUT) with the test pattern defined by

$$DATA(R, C) = \{(R + SEED), (C + SEED)\}, \quad (1)$$

where $SEED$ is a test parameter, R is the Row address, and C is the Column address. After the writing operation, the value of some randomly chosen spy cells of the HDUT is corrupted and the device undergoes a preliminary test routine to validate the correct behavior of the write and the read operations verifying that the differences between the values of the HDUT and the CDUT cells correspond only to those of the spy cells. If this operation succeeds, then the refresh is stopped until the Discharge Time (DT) is elapsed. At that time, the refresh procedure is restarted and the test routine is performed again to count the cells that lose the stored information after DT. Then DT is incremented of DTS (DT Step) and if DT is still less than a predefined value DT-MAX, a new test procedure is performed. The Test Cycle procedure collects the data to characterize the device at a certain value of total dose, as shown in Fig. 4. At this point,

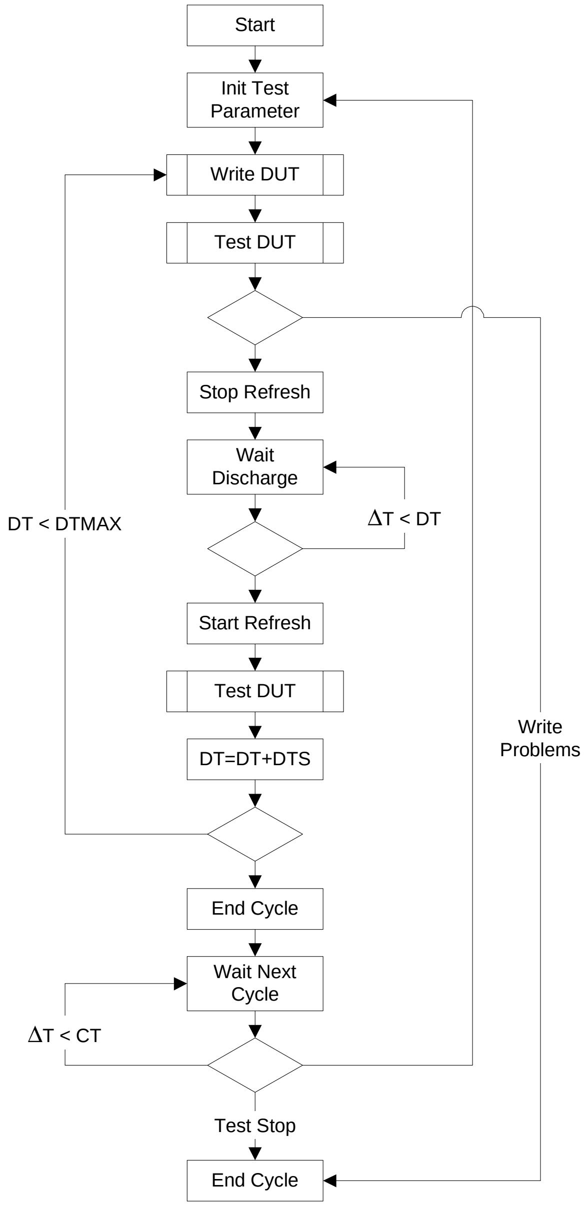

Figure 1. Test flow

1 Panoramic Gammabeam model 150A produced by Nordion Ltd (Canada), with an activity 1500 Ci. This equipment, owned by CNR (National Research Council of Italy), is usually devoted to studies of polymerization, degradation of polymers induced by ionizing radiation, and radiation effects in materials for industrial applications. In particular, the dose rate characteristics (0.01-10 rad(Si)/s) are suitable for total dose tests on electronic components for space applications. The geometry of the radiation field intensity, known from manufacturer's maps, has been experimentally verified at various distances from the source by the Fricke dosimeter technique.

the Test Cycle procedure is suspended and the device accumulate TID for a time CD (Cycle Delay) in realistic refresh conditions. The test stops at the end of the irradiation.

The TID effects on Micron 256 Mb SDRAM devices have been investigated. In particular, MT48LC32M8A2Y96A dies directly bonded onto suitable carriers, have been used. Overall, four devices have been radiated. Two of them have been constantly keep under operation, while the other two have been radiated and characterized only before and after the exposure. The test consisted of two sequential irradiation sessions of 50 krad and 20 krad respectively for a total dose of 70 krad and monitoring the exposed memory cells logic state measuring the number of cells which shown a logic state change vs. the latency time, that is the time between the cell write operation and the following reading of their value, in the range between about 50 ms and about 30 s. This test has been performed during the exposure at regular predefined dose intervals (about 10–15 krad).

In order to test SDRAM cells, a custom Test Board, shown in Fig. 2, has been developed and implemented. In order to achieve the maximum performance allowed by the SDRAM advanced input-output features (burst mode, self refresh), the Test Board (TB) was developed using a FPGA. The system core mapped on the FPGA is the Memory Control module that is able to handle read, write and refresh operations plus complex test procedures as:

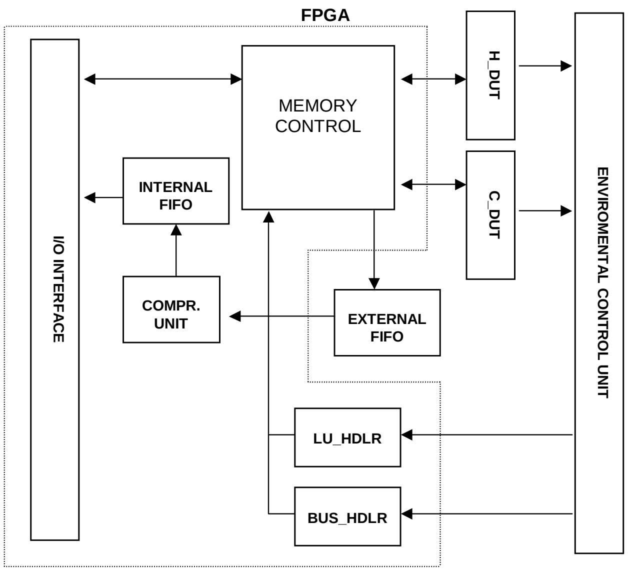

Figure 2. Test Board scheme

- Write an internally generated pattern on block cell.
- Read a block of cells.
- Compare a block of cells.

The compare operation is the basis for all the test procedures; in fact the status of the DUT (Hot-DUT) is checked by comparing the content of its cells with the corresponding ones of a reference device (Cold-DUT). The results of the compare operation, which is performed in burst mode at the full speed of the hardware, are stored in a FIFO; a compression procedure is then performed in order to transmit only the information on the differences to the Test Control PC (TCPC). The communication between TB and TCPC is obtained by a Client-Server scheme, which allows TCPC to remotely drive the test. The RABBIT microprocessor is connected to the TB I/O interface and supports TCP-IP Ethernet connection towards TCPC (Fig. 3). A dedicated software is loaded in the microprocessor flash Memory to manage the communication on TCP-IP protocol and to correctly drive the TB.

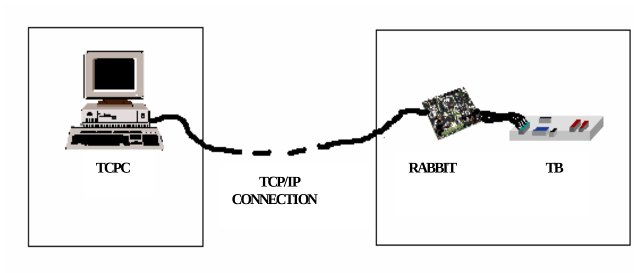

Figure 3. TCI-IP connection

3. Results

The analysis of the test data emphasizes the following interesting effects.

1. A gradual reduction of the data retention time proportional to the absorbed dose (Fig. 4 and 5). This evident effect allows us to establish a direct relation between the number of the errors and the absorbed dose (Fig. 6).
2. An immediate increase of the number of errors during irradiation (Fig. 5, curve 50 krad Off e 50 krad On). This effect originates from charge injection in the depletion regions by incident ionizing radiation, which produces leakage currents that alters the amount of charge and hence the cell state. Moreover, this effect suggests a method for dose rate measurements.
3. An annealing effect that causes a noticeable degradation of the performance of the devices during the their life (Fig. 7).

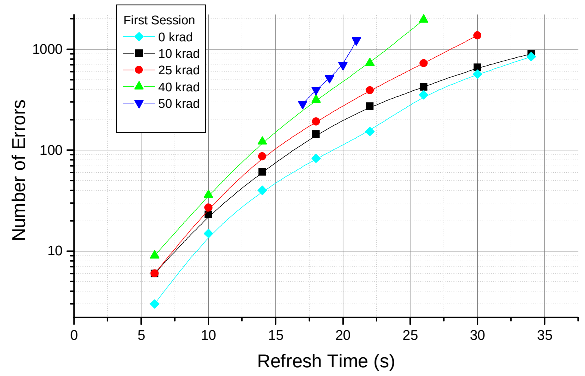

Figure 4. Number of errors vs. the refresh time in the 1st test session (0-50 krad)

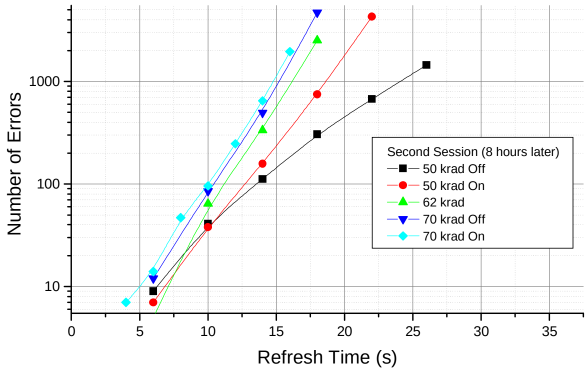

Figure 5. Number of errors vs. the refresh time in the 2nd test session (50-70 krad)

4. At last, comparing the data with those measured after 72 h the exposure (Fig. 8), clearly shows the decisive role of the bias voltages applied to the device during the exposure. In fact, because the voltages hinder the recombination of the $e - h$ couples produced in the device by the radiation, they amplify the radiation effects.

4. Conclusions

The paper proposes a novel online monitoring method to measure the degradation of SDRAM devices due to Total Ionizing Dose based on the measurement of the bit retention time.

The experimental setup and the results of a preliminary TID test with a ^{60}Co gamma ray source on SDRAM are presented. In particular, the analysis of the test data shows a linear reduction of the data retention time proportional to

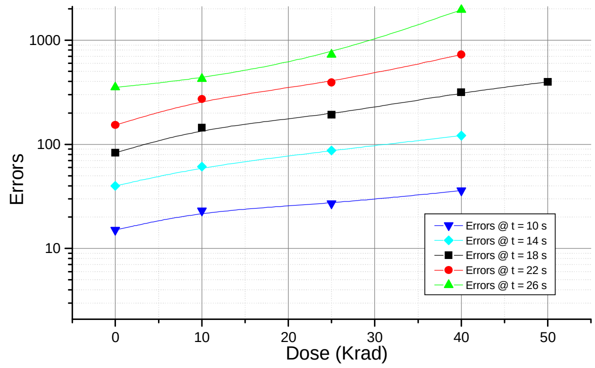

Figure 6. Relation between the number of errors and the absorbed dose for different latency time

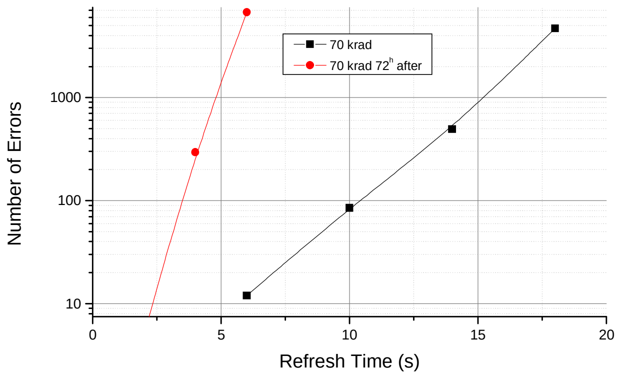

Figure 7. Device degradation due to the annealing

the absorbed dose. It is important to note that for small absorbed dose levels, although the device maintains the correct behavior in nominal conditions, this method allows us to measure the effect of the radiation.

Moreover, because of high sensitiveness of this method, the described approach could be used to compute also the absorbed dose starting from the number of the corrupted memory cells.

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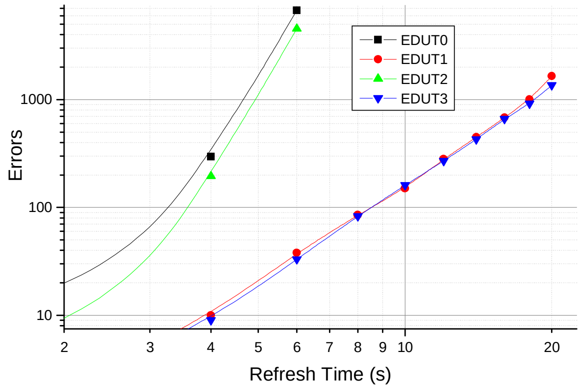

Figure 8. Bias voltage effect during the exposure

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