

Reduced complexity full-flash ADCs.

Roberto Lojacono

Università di Roma "Tor Vergata"- Dip. DIE
Viale del Politecnico, 1 - 00133 - Roma - Italy
Ph. ++39 06 72597494 - Fax ++39 06 2020519
e-mail lojacono@uniroma2.it

Abstract- This paper presents innovative schemes of "full-flash" and "subranging" A/D converter architectures. These new architectures are based on a conversion technique inferred by an electrical interpretation of the calliper rule. This kind of ADC implementation allow the dramatic reduction of the required resistors. Indeed, while a traditional full-flash or subranging ADC requires a voltage comparison scale realized by a series of 2^n resistors, being n the number of bits of the resulting binary samples, the proposed architectures require only $3 \cdot 2^{n/2}$ resistors. This reduction produces an obvious advantage in general case but can render possible the realization of full-flash ADC of large word lengths.

I. Introduction

A traditional full-flash ADC requires a reference voltage scale realized by a series of a great number of resistors, namely 2^n if n is the required word length. This number of resistors limits the practical implementation of these converters to 10 bits or minus. Indeed the allocation of a great number of resistors into a single chip creates a lot of problems. Random mismatch between monolithically integrated resistors is inversely proportional to the square root of their area while systematic mismatch due to process gradients increases with their area and separation. For a BiCMOS process, total resistor area should be less than about $10,000 \mu\text{m}^2$ to avoid gradient errors [1]. On the other hand, individual resistor areas must be well over $100 \mu\text{m}^2$ to obtain low random error. The resistor area versus matching trade-off is such that good matching of many resistors covering an area of the order of a square millimetre cannot be obtained if only first-order gradients are cancelled [2]. These constraints discourage the design of large word length full-flash ADC's. However, also the most used subranging architectures, realized having the main purpose of reducing the number of comparators, require a voltage reference scale.

This paper presents a new kind of architecture in which the reference voltage steps are realized by a technique derived from the calliper rule. This technique implements a "virtual" fine reference voltage scale obtained by comparison between two scales having coarse steps. In this way the required resistors for an n -bits conversion word length are reduced to $3 \cdot 2^{n/2}$.

II. Proposed architecture

The proposed technique was already presented by the author [3]. Here are briefly reported, for the sake of clarity, the useful features of this technique which are used for the proposed architecture.

A simple example of classical subranging architecture is given in fig. 1-a [3]. The circled switches must be closed to obtain the correct output corresponding to the .8 V of the input. The comparators outputs form a thermometer-like scale that must be converted in binary by a suitable encoder. Here a cascade of resistors furnishes a scale of fine reference voltage values. Some of these voltages, having equal coarse spacing between them, are used for a coarse conversion. A set of comparators form a thermometer like scale, which gives the coarse output to be encoded in binary (MSB). A multiplexer, driven by the coarse output, select the proper reference voltages for a second fine stage. Again, a set of comparators form a thermometer like scale, which gives the fine output to be encoded in binary (LSB). The proposed architecture (fig. 1-b) make use of two scales: a fixed one and a mobile one, as in the calliper.

The mobile scale is driven by the input voltage by means of two op-amps. To explain the proposed realization technique, firstly we recall the calliper properties. In the calliper, the two scales are determined in such a way that the same interval l (length in the calliper, voltage in our case) is divided by n in the fixed scale and by $1 + n$ in the mobile one. Usually, in the calliper, l/n is the coarse unity, ($l = 19\text{mm}$ and $n = 19$), so $1/20$ of the coarse unity ($= 1/20\text{mm}$) can be resolved. The result X of the measure is given by:

$$X = \frac{l}{n} \cdot \left(k_1 + \frac{1}{n+1} \cdot k_2 \right) \quad (1)$$

Where k_1 is the number of integer mm s, i.e. the number of marks of the fixed scale involved in the translation of the origin of the mobile scale, and k_2 the number of marks in the mobile scale between

III. Integration of the proposed architecture in the sample-hold circuit

The proposed architecture can be integrated in the sample-hold circuit [4], as explained in the following. A schematic diagram of a simple track and hold circuit is given in figure 3.

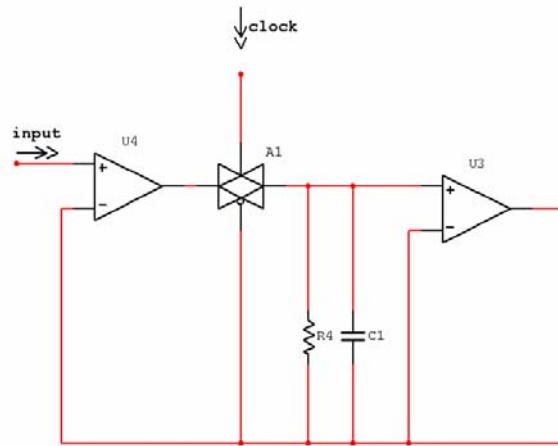


Figure 3. Schematic diagram of a simple track and hold circuit.

Figure 4 shows how the proposed architecture can be included in the sample-hold circuit, thus reducing the delay introduced by the OP-AMP. Here the “mobile” scale is driven by only one OP-AMP. The required voltage across this scale is furnished by a separate source, which can be also external.

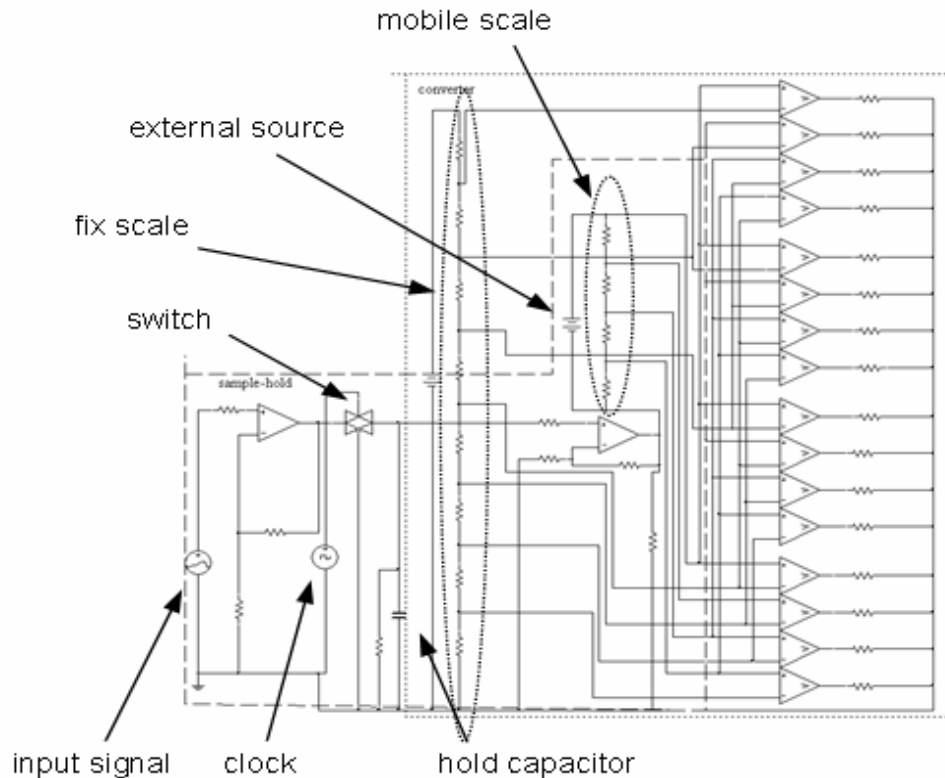


Figure 4. The proposed technique applied to a 4-bits full-flash converter. The “mobile” scale is driven by an external source. The proposed architecture is integrated in the track and hold circuit.

The effect of the integration of the proposed architecture in the track and hold circuit is that the held signal is split in several levels by the “mobile” scale. These levels are compared with the levels of the “fix” scale by the comparators which realize the thermometric scale. When two levels of the two scales coincide, a comparator changes state. This dynamical behaviour is illustrated in figure 5, which reports the result of a transient SPICE simulation of the circuit of figure 4. Here, we can observe the clock signal (vertical nearer lines), the ramp input signal, its sampled version, given by the track and hold circuit, and the replica of this sampled version given by the “mobile” scale. The horizontal lines represent the voltage levels of the “fix” scale. The changes of the state of the comparators appear as far vertical lines.

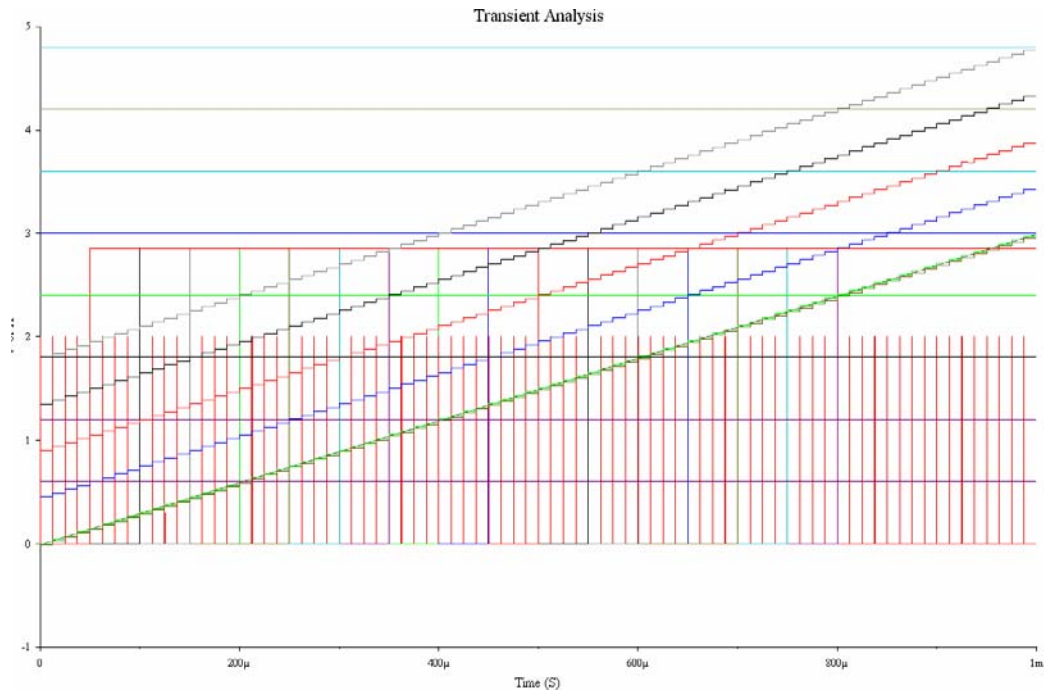


Figure 5. Transient simulation of the behaviour of the circuit of figure 4 when the input signal is a ramp voltage.

IV. Conclusions

A innovative architecture of full-flash or subranging ADC has been presented. This architecture reduces dramatically the number of the required resistors in the reference voltage scale. This means that the complexity of the whole structure of the ADC can be reduced thus allowing the possibility of realizing great word length converters. SPICE simulations shown that this kind of architectures is valid in principle. Work is in progress in realizing a complete layout of a whole converter and in quantifying the related conversion accuracy.

References

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