

# FPGA Implementation of a Fast Hardware Architecture for Medical Digital Image Processing

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## I. INTRODUCTION

In order to increase radiologists diagnostic performance, several computer-aided diagnosis (CAD) schemes have been developed in the last years to improve the detection of primary signatures of many disease, such as masses and microcalcifications in mammograms. Owing to the huge variability of the features to be detected in such images, very specific algorithms have to be studied in order to perform a correct processing, increasing the readability of the image itself without introducing artifacts. In particular, image processing in the wavelet domain shows very appealing characteristics, because the wavelet transform permits to detect details appearing at different scales and selectively enhance them within different resolution levels [1]. In particular, wavelet orthogonal and biorthogonal bases have been successfully used in many applications. It has already been stressed that the lack of translation invariance of these representations can be a severe drawback because leads to the introduction of a large number of artifacts in the synthesis coefficients. We refer, for example, to pseudo-Gibbs phenomena in the neighbourhood of discontinuities [4]. The *Dyadic Wavelet Transform* [5]–[8] pioneered by Mallat and Zhong was precisely introduced to cope with this. It provides a redundant representation, so that exhibits translation invariance and in [9] it was shown that using undecimated transform rather than decimated ones can improve the results of denoising more than 2.5. That undecimated decomposition is computed using the same filter-bank of a bi-orthogonal wavelet transform and each band has the same size as the original image. The general scheme for wavelet-based image enhancement is the following: 1) wavelet decomposition; 2) modification of wavelet coefficients at various scales; 3) image reconstruction starting from modified coefficients. In this work we use, as a redundant representation, the discrete dyadic transform introduced in [5], that can be implemented within the hierarchical filtering scheme shown in Fig. 1(a), in which are highlighted the points at which the denoising and enhancement [2], [3] are inserted. Filters

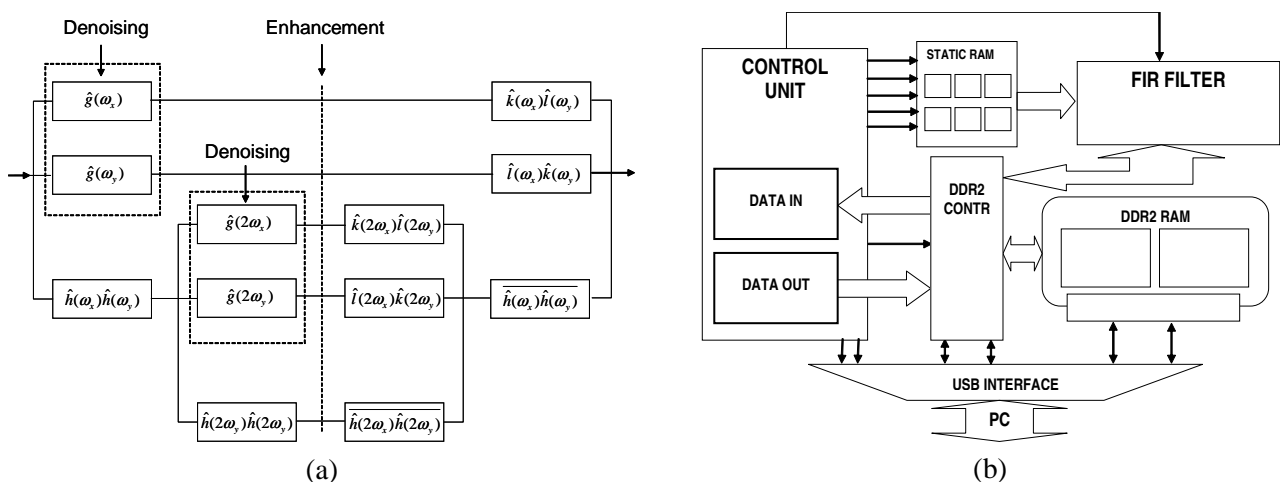


Fig. 1. (a) 2D dyadic wavelet transform (two levels shown) and (b) scheme of the HW implementation.

definition can be found in [6]–[8]. Unfortunately, owing to the large size of medical images (often many millions of pixels) and the large number of coefficients to be handled, the whole computation time does not allow a fast processing.

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## II. A FAST HARDWARE IMPLEMENTATION

The aim of the work is the implementation in hardware of the dyadic undecimated wavelet transform core. In fact, an hardware architecture allows us to drastically reduce decomposition, handling of coefficients, and reconstruction times with respect to a software implementation. This is due to the large parallelism we can realize in hardware, while in software the algorithm progress is coerced by the intrinsic serial microprocessor architecture, the delays due to data interchange between the CPU, memory and peripherals, and at last by the other processes running on the system. The original 12-bit gray map image is subdivided into  $512 \times 512$  pixel windows, and each window is separately processed one row and one column at time. The scheme of the HW implementation is shown in Fig. 1(b). The core of the hardware architecture includes a FIR filter with configurable taps for each level and for each filter type. The number of taps, whose coefficients are stored in the static RAM, equals to the longer used filter. To fill the delay line of each filter it has been used the circular convolution that permits the optimal reconstruction of the original image. The IN memory controller loads the filter coefficients while the OUT memory controller stores the decomposed images. These controllers emulate the convolution procedure loading data in the proper way through a programmed memory pointer. The main memory is a very fast DDR2 RAM, controlled by a suitable designed device. An USB controller realizes the data transfer between the board and the PC. A main control unit administrates all the operations of the whole processing. The performance of the algorithm has been studied taking into account the fixed arithmetic and the system has been designed in Verilog and mapped on the Altera test board Video Development Kit Cyclone II Edition based on FPGA Cyclone II EP2C70F672C6. The arithmetic operation runs at 250 MHz, while the frequency of the RAM is 167 MHz and the data transfer rate of the USB interface is 100 Mbit/s. The time to process a whole  $512 \times 512$  pixel images is less than 0.35 s (about 0.01 times the time of a software implementation). In Fig. 2 some simulation results obtained during the board design with Active-HDL software are shown.

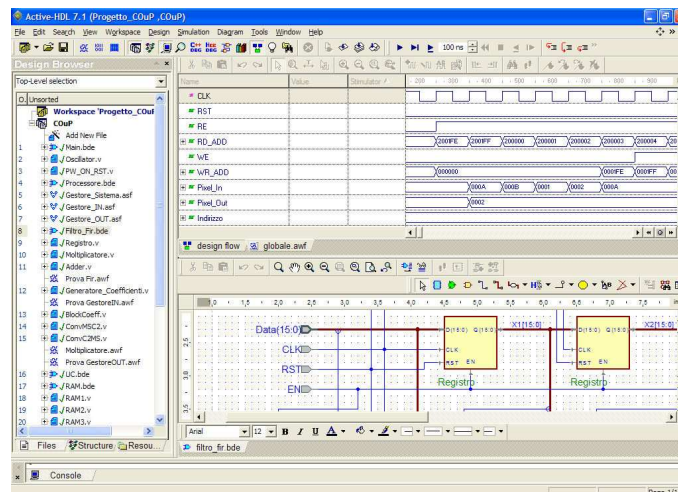


Fig. 2. Simulation results obtained during the board design

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